

ABSTRACT OF THE DISCLOSURE

A silicon carbide n channel MOS semiconductor device is provided which includes a silicon carbide substrate including a p base region, an n⁺ source region and an n⁺ drain region, a gate insulating film formed on a surface of the p base region, a gate electrode provided on the gate insulating film, and first and second main electrodes that allow current to flow therebetween, wherein a p⁻ channel region is formed in a surface layer of the p base region right under the gate insulating film, such that the effective acceptor concentration measured in the vicinity of an interface between the p base region and the gate insulating film is in a range of 1×10^{13} to $1 \times 10^{16} \text{ cm}^{-3}$. A method for manufacturing such a MOS semiconductor device is also provided in which the p⁻ channel region is formed by conducting multiple ion implantation in which the amount of ions to be implanted is reduced in the vicinity of the surface of the p base region, or implanting ions of donor impurities into a surface layer of the p base region, or forming a low-concentration layer by epitaxial growth as a surface layer of the p base region.